CY2542

Quad-PLL Programmable Spread Spectrum Clock Generator with Two-Wire Serial Interface and Frequency Select

Features

- Device operating voltage option:1.8 V
- Selectable clock output voltages:
  - 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V
- Fully integrated ultra low-power phase-locked loops (PLLs)
- Input reference clock frequency range:
  - External crystal: 8 to 48 MHz
  - External reference: 1 to 48 MHz clock
- Output clock frequency range:
  - 3-50 MHz for 1.5 V/1.8 V output voltage
  - 3-166 MHz for 2.5 V/3.0 V/3.3 V output voltage
- Up to eight programmable output clocks through two-wire serial interface
- Programmable output drive strengths
- Frequency select feature with option to select four different clock Frequencies over eight clock outputs
- 150 ps typical cycle-to-cycle jitter
- 24-pin QFN (4 × 4 × 0.6 mm) Package
- Commercial temperature range
- One-time programmability
  For programming support, contact Cypress technical support or send an e-mail to clocks@cypress.com

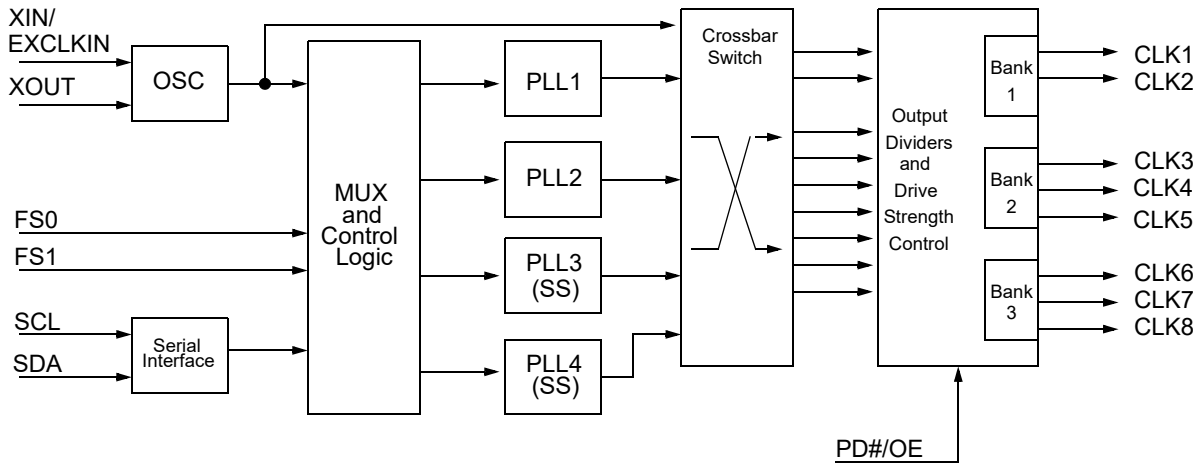
Benefits

- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific programmable EMI reduction using Spread Spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of zero PPM frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low-power systems

Functional Description

For a complete list of related documentation, click here.

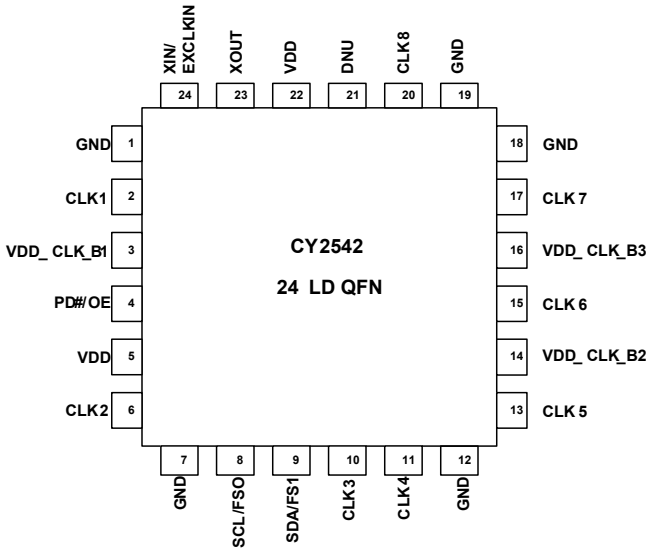
Logic Block Diagram



Contents

Pinouts

Figure 1. 24-pin QFN pinout



Pin Definitions

(V_{DD} = 1.8 V Supply)

Pin Number	Name	I/O	Description
1	GND	Power	Power supply ground
2	CLK1	Output	Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B1}$ voltage
3	$V_{DD\_CLK\_B1}$	Power	Power supply for Bank1 (CLK1, CLK2) outputs: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
4	PD#/OE	Input	Multifunction programmable pin: Output enable or power down modes
5	V_{DD}	Power	Power supply: 1.8 V
6	CLK2	Output	Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B1}$ voltage
7	GND	Power	Power supply ground
8	SCL/FS0	Input	Multifunction programmable pin: Serial data clock or Frequency select input pin
9	SDA/FS1	Input/Output	Serial data input/output or Frequency select input pin
10	CLK3	Output	Programmable clock output with no spread spectrum. Output voltage depends on $V_{DD\_CLK\_B2}$ voltage
11	CLK4	Output	Programmable clock output with no spread spectrum. Output voltage depends on $V_{DD\_CLK\_B2}$ voltage
12	GND	Power	Power supply ground
13	CLK5	Output	Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B2}$ voltage
14	$V_{DD\_CLK\_B2}$	Power	Power supply for Bank2 (CLK3, CLK4, CLK5) outputs: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
15	CLK6	Output	Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B3}$ voltage
16	$V_{DD\_CLK\_B3}$	Power	Power supply for Bank3 (CLK6, CLK7, CLK8) outputs: 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V
17	CLK7	Output	Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B3}$ voltage
18	GND	Power	Power supply ground
19	GND	Power	Power supply ground
20	CLK8	Output	Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B3}$ voltage
21	DNU	None	Do not use
22	V_{DD}	Power	Power supply: 1.8 V
23	XOUT	Output	Crystal output
24	XIN/EXCLKIN	Input	Crystal Input or 1.8 V external reference clock input

Functional Overview

Four Configurable PLLs

The CY2542 is a four-PLL clock generator IC. It can be used to generate four independent output frequencies ranging from 3 to 50 MHz (for 1.5 V/1.8 V output voltage) or 3-166 MHz (for 2.5 V/3.0 V/3.3 V output voltage) from a single crystal or a reference clock.

Two-wire Serial Interface Programming

The CY2542 has a two-wire serial interface that programs the configuration memory array to synthesize output frequencies by programmable output divider, spread characteristics, and drive strength. Two-wire Serial Interface can also be used for in-system control of these programmable features.

Input Reference Clocks

The input to the CY2542 can be either a crystal or a clock signal. The input frequency range for crystals is 8 MHz to 48 MHz, while that for EXCLKIN is 1 to 48 MHz. The voltage level for the input reference clock used must meet the voltage requirement for the device as shown in the DC and AC specifications.

Output Power Supply Options

The CY2542 has eight clock outputs grouped in three banks. The Bank 1, Bank 2, and Bank 3 correspond to (CLK1, CLK2), (CLK3, CLK4, CLK5), and (CLK6, CLK7, CLK8) respectively. A separate power supply is used for each of these three output drivers and they can be any of 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V giving user multiple choice of output clock voltage levels.

Output Source Selection

The CY2542 has eight clock outputs (CLK1–8). There are five available clock sources for these outputs. These clock sources are: XIN/EXCLKIN, PLL1, PLL2, PLL3 and PLL4. Output clock source selection is done using four out of five crossbar switch. Thus, any one of these five available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to four independent clock and a reference clock outputs.

Spread Spectrum

Two of the four PLLs (PLL3 and PLL4) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the PLL. It can be factory programmed to either center spread range from ±0.125% to ±2.50%, or down spread range from –0.25% to –5.0%, with Lexmark or Linear modulation profile.

Frequency Select

There are two multifunction frequency select pins (FS0, FS1) that provide an option to select four different sets of frequencies among each of the four PLLs. Each output has programmable output divider options.

Glitch-Free Frequency Switch

When the frequency select pin (FS) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is being switched.

PD#/OE Mode

PD#/OE input (Pin 4) can be programmed to operate as either power down (PD#) or output enable (OE) mode. Note that power down shuts off the entire chip, resulting in minimum power consumption for the device. Setting this signal high brings the device in the operational mode with default register settings. The PD# turn-on time is limited by the turn-on time of the PLLs. Disabled outputs are first driven to a low state before turning off. When off, they are held low by internal weak resistors (~160 k ohms)

When this pin is programmed as output enable (OE), clock outputs can be enabled or disabled using OE (pin 4). Individual clock outputs can be programmed to be sensitive to this OE pin.

Keep Alive Mode

By activating the device in the Keep Alive Mode, power down mode is changed to power saving mode, which disables all PLLs and outputs, but preserves the contents of the volatile registers. Thus, any configuration changes made via two-wire serial interface are preserved. By deactivating the Keep Alive Mode, changes made due to serial interface is not preserved during power down, but power consumption is reduced relative to the Keep Alive Mode.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 1 shows the typical rise and fall times for different drive strength settings.

Table 1. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	6.8
Mid Low	3.4
Mid High	2.0
High	1.0

Factory Specific Configuration and Custom Programming

The device is available with factory specific programmed frequencies as shown in the Ordering Information page. This factory specific programmed part can be used for the device evaluation purposes. The CY2542 can be custom programmed to any desired frequencies and listed features. For customer specific programming and two-wire Serial Interface programmable memory bitmap definitions, contact your local Cypress Field Application Engineer (FAE) or sales representative.

Two-wire Serial Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. This interface is used to write (and optionally read) control registers that control various device functions such as enabling individual clock output buffers. The registers initialize to their default setting upon power up and therefore, use of this interface is optional. Clock device registers are normally changed upon system initialization. Any data written via serial interface is volatile and is not retained when the device is powered down.

The two-wire serial interface uses two signals, SDA and SCL, that operates up to 400 kbits/s in Read or Write mode. The SDA and SCL timing and data transfer sequence is shown in Figure 2. The basic Write serial format is as follows:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit. The basic serial format is illustrated in Figure 3.

Figure 2. Data Transfer Sequence on the Serial Bus

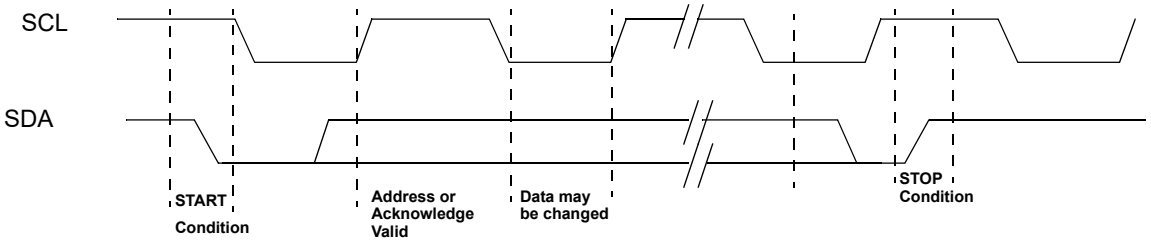
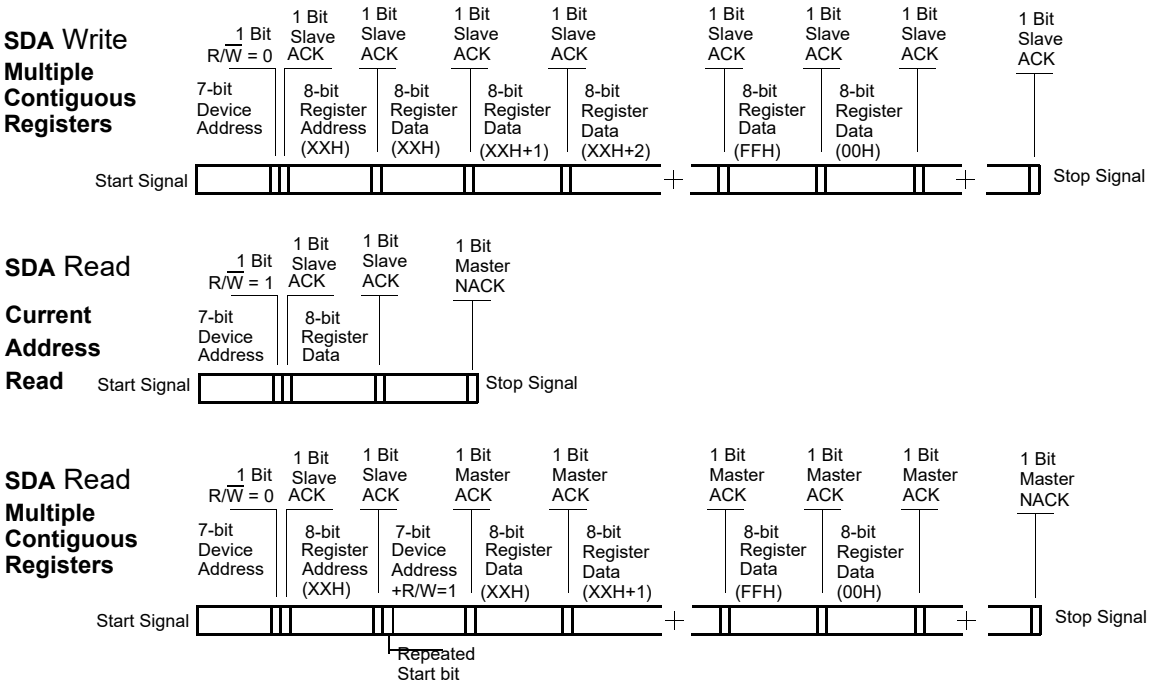


Figure 3. Data Frame Architecture



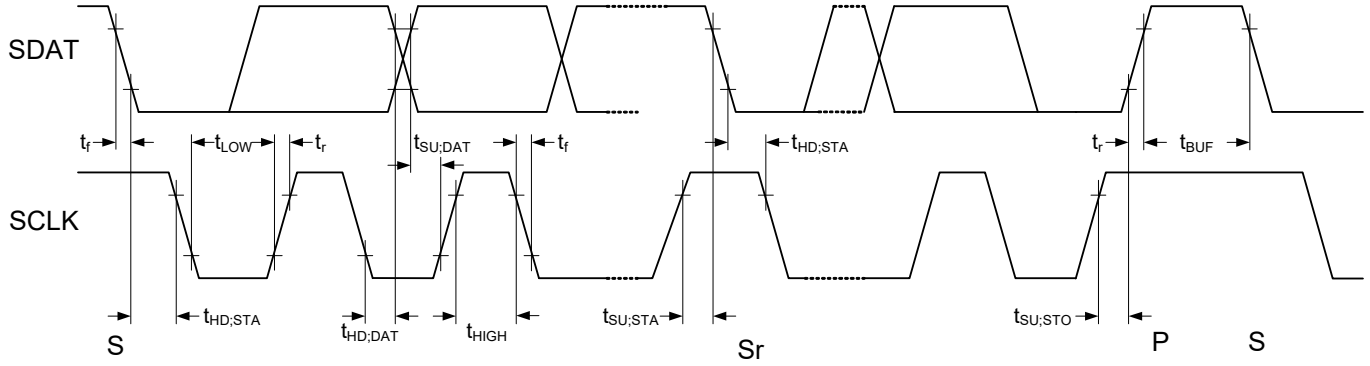
Device Address

The device serial interface address is 69H. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

Data Valid

Data is valid when the clock is HIGH, and can only be transitioned when the clock is LOW, as illustrated in Figure 4.

Figure 4. Data Valid and Data Transition Periods



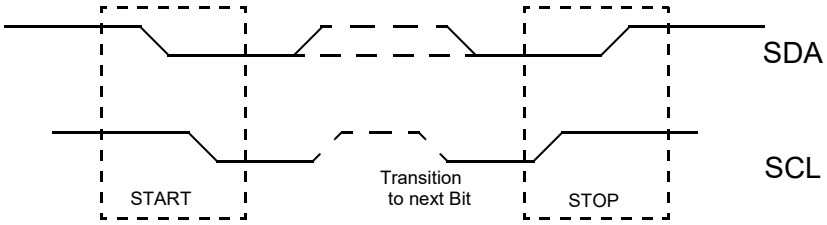
Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 5.

Start Sequence – SDA going LOW when SCL is HIGH indicates a Start Frame. Every time a start signal is supplied, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by register address (eight bits) and register data (eight bits).

Stop Sequence – SDA going HIGH when SCL is HIGH indicates a Stop Frame. A Stop Frame frees the bus to write to another part on the same bus or to write to another random register address.

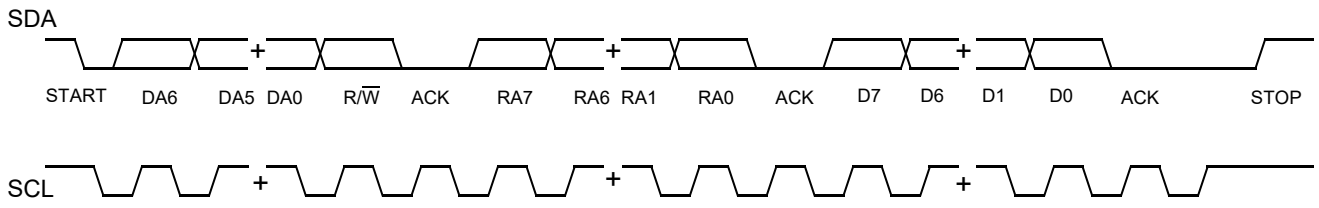
Figure 5. Start and Stop Frame



Acknowledge Pulse

During Write Mode, the CY2542 responds with an Acknowledge pulse after every eight bits. This is done by pulling the SDA line LOW during the N*9th clock cycle, as illustrated in Figure 6 (N = the number of bytes transmitted). During Read Mode, the master generates the acknowledge pulse after reading the data packet.

Figure 6. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (ACK = 0/LOW). The next eight bits must contain the data word intended for storage. After receiving the data word, the slave responds with another acknowledge bit (ACK = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write multiple bytes at a time, the master must not end the write sequence with a STOP condition, but instead sends multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, the same as after the first byte, and accepts data until the acknowledge bit is responded to by the STOP condition. When receiving multiple bytes, the CY2542 internally increments the register address.

Read Operations

Read operations are initiated the same way as Write operations except that the R/W bit of the slave address is set to '1' (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY2542 has an onboard address counter that retains '1' more than the address of the last word accessed. If the last word written or read was word 'n', then a current address read operation returns the value stored in location 'n+1'. When the CY2542 receives the slave address with the R/W bit set to a '1', it issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes CY2542 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first set the word address. To do this, send the address to the CY2542 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to '1'. The CY2542 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the CY2542 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action increments the internal address pointer, and subsequently outputs the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master serially reads the entire contents of the slave device memory. When the internal address pointer points to the FFH register, after the next increment, the pointer points to the 00H register.

Serial I^2C Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	Frequency of SCLK	–	400	kHz
$t_{HD:STA}$	Hold time START condition	0.6	–	µs
t_{LOW}	Low period of the SCLK clock	1.3	–	µs
t_{HIGH}	High period of the SCLK clock	0.6	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	0.6	–	µs
$t_{HD:DAT}$	Data hold time	100	–	ns
$t_{SU:DAT}$	Data setup time	100	–	ns
t_R	Rise time	–	300	ns
t_F	Fall time	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	0.6	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	1.3	–	µs

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	–	–0.5	2.8	V
V_{DD_CLKX}	Supply voltage	–	–0.5	4.4	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	2.2	V
T_S	Temperature, storage	Non functional	–65	+150	°C
ESD_{HBM}	ESD protection (human body model)	JEDEC EIA/JESD22-A114-E	2000	–	V
UL-94	Flammability rating	V-0 @1/8 in.	–	10	ppm
MSL	Moisture sensitivity level	–	3		

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	V_{DD} operating voltage	1.65	1.80	1.95	V
$V_{DD\_CLK\_BX}$	Output driver voltage	1.43	–	3.60	V
C_{LOAD}	Maximum load capacitance	–	–	15	pF
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms
T_A	Ambient temperature, commercial	0	–	70	°C

DC Electrical Specifications

($V_{DD\_CLK\_BX}$ = 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	Output low voltage, CLK pins	I_{OL} = 2 mA, drive strength = [00]	–	–	0.4	V
		I_{OL} = 3 mA, drive strength = [01]				
		I_{OL} = 7 mA, drive strength = [10]				
		I_{OL} = 12 mA, drive strength = [11]				
V_{OH}	Output high voltage, CLK pins	I_{OH} = –2 mA, drive strength = [00]	$V_{DD\_CLK\_BX}$ – 0.4	–	–	V
		I_{OH} = –3 mA, drive strength = [01]				
		I_{OH} = –7 mA, drive strength = [10]				
		I_{OH} = –12 mA, drive strength = [11]				
V_{OLSD}	Output low voltage, SDA	I_{OL} = 4 mA	–	–	0.4	V
V_{IL1}	Input low voltage of PD#/OE, SDA and SCL pins		–	–	0.2 × V_{DD}	V
V_{IL2}	Input low voltage of EXCLKIN pin		–	–	0.2 × V_{DD}	V
V_{IH1}	Input high voltage of PD#/OE, SDA and SCL pins		0.8 × V_{DD}	–	2.2	V
V_{IH2}	Input high voltage of EXCLKIN pin		0.8 × V_{DD}	–	2.2	V
I_{IL1}	Input low current, PD#/OE pin	V_{IL} = 0 V	–	–	10	µA
I_{IH1}	Input high current, PD#/OE pin	V_{IH} = V_{DD}	–	–	10	µA
R_{DN}	Pull-down resistor of clocks (CLK1-CLK8) in off-state	Clock outputs in off-state by setting PD# = Low	100	160	250	kΩ
I_{DD}[1, 2]	Supply current	All outputs running, C_{LOAD} = 0	–	15	–	mA
I_{DDS}[1]	Standby current	PD# = Low, and serial interface circuit not in Keep Alive Mode	–	3	–	µA
C_{IN}[2]	Input capacitance	SCL, SDA and PD#/OE inputs	–	–	7	pF

Notes
1. This parameter is configuration dependent. The specified value is for the drive level setting of [1,1].
2. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.

AC Electrical Specifications

($V_{DD\_CLK\_BX}$ = 1.5 V/1.8 V/2.5 V/3.0 V/3.3 V)

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{CLK}	Clock output frequency	All clock outputs (for 1.5 V/1.8 V output voltage)	3	–	50	MHz
F_{CLK}	Clock output frequency	All clock outputs (for 2.5 V/3.0 V/3.3 V output voltage)	3	–	166	MHz
F_{REF} (crystal)	Crystal frequency, XIN	–	8	–	48	MHz
F_{REF} (clock)	Input clock frequency, EXCLKIN	–	1	–	48	MHz
DC	Output clock duty cycle	Duty Cycle is defined in Figure 8 on page 13; t_1/t_2, measured at 50% of $V_{DD\_CLK\_BX}$	45	50	55	%
T_{RF1}[4]	Output clock rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 9 on page 13, C_{LOAD} = 15 pF, drive strength [00]	–	6.8	10.0	ns
T_{RF2}[4]	Output clock rise/fall time	Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 9 on page 13, C_{LOAD} = 15 pF, drive strength [01]	–	3.4	5.0	ns
T_{RF3}[4]	Output clock rise/fall time	Measured from 20% to 80% of $V_{DD\_CLKX\_BX}$, as shown in Figure 9 on page 13, C_{LOAD} = 15 pF, drive strength [10]	–	2.0	3.0	ns
T_{RF4}[4]	Output clock rise/fall time	Measured from 20% to 80% of $V_{DD\_CLKX\_BX}$, as shown in Figure 9 on page 13, C_{LOAD} = 15 pF, drive strength [11]	–	1.0	1.5	ns
T_{CCJ}[3, 4]	Cycle-to-cycle jitter	EXCLKIN = CLKx = 48 MHz, C_{LOAD} = 15 pF, 4 PLLs and 1 output for each PLL enabled, drive strength = [11]	–	150	–	ps
T_{LOCK}[4]	PLL Lock time	–	–	1	3	ms

Notes
3. This parameter is configuration dependent. The specified value is for the drive level setting of [1,1].
4. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.

Recommended Crystal Specification

For SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
MO	Mode of operation		Fundamental		
Fmin	Minimum frequency	8	14	28	MHz
Fmax	Maximum frequency	14	28	48	MHz
R1	Motional resistance (ESR)	135	50	30	Ω
C0	Shunt capacitance	4	4	2	pF
CL	Parallel load capacitance	18	14	12	pF
DL(max)	Maximum crystal drive level	300	300	300	µW

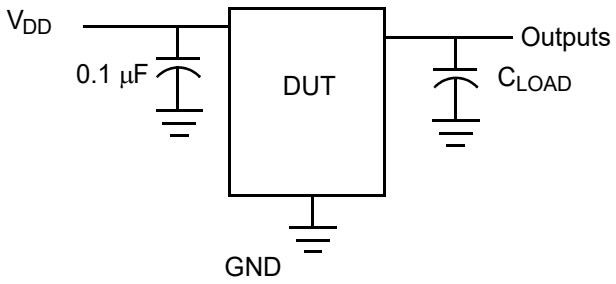
Recommended Crystal Specification

For Thru-Hole Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
MO	Mode of operation		Fundamental		
Fmin	Minimum frequency	8	14	24	MHz
Fmax	Maximum frequency	14	24	32	MHz
R1	Motional resistance (ESR)	90	50	30	Ω
C0	Shunt capacitance	7	7	7	pF
CL	Parallel load capacitance	18	12	12	pF
DL(max)	Maximum crystal drive level	1000	1000	1000	µW

Test and Measurement Setup

Figure 7. Test and Measurement Setup



Voltage and Timing Definitions

Figure 8. Duty Cycle Definition

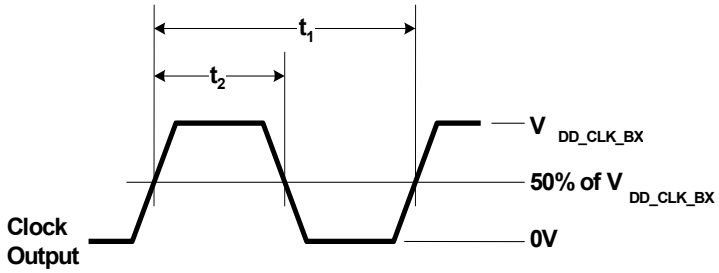
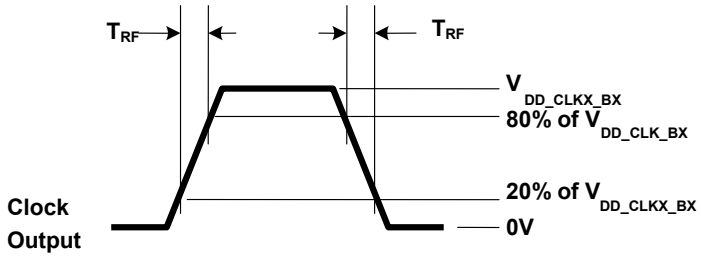


Figure 9. Rise Time = T_{RF}, Fall Time = T_{RF}



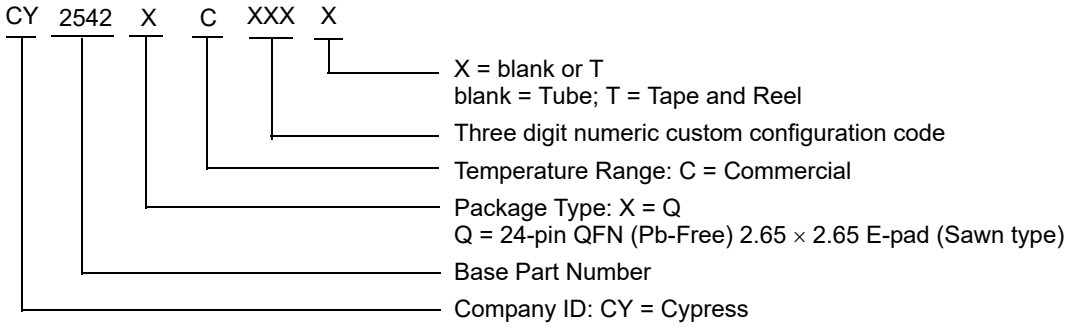
Ordering Information

All product offerings are factory programmed customer specific devices with customized part numbers. Table 2 shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Table 2. Possible Configurations

Part Number[5]	Type	V_{DD} (V)	Production Flow
Pb-free			
CY2542QCxxx	24-pin QFN	V_{DD} = 1.8 V $V_{DD\_CLK\_Bx}$ = 1.5/1.8/2.5/3.0/3.3 V	Commercial
CY2542QCxxxT	24-pin QFN - Tape and Reel	V_{DD} = 1.8 V $V_{DD\_CLK\_Bx}$ = 1.5/1.8/2.5/3.0/3.3 V	Commercial

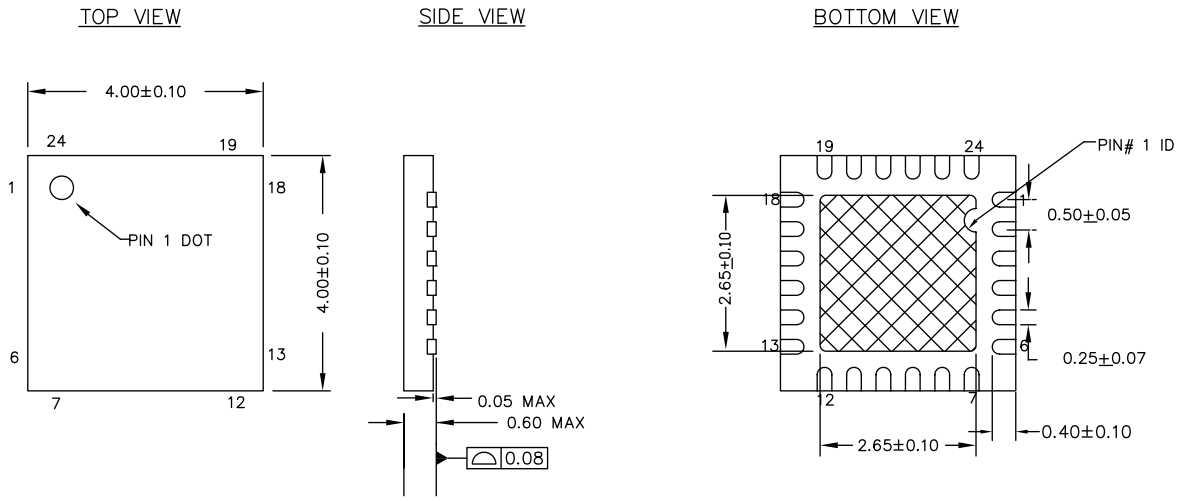
Ordering Code Definitions



Note
5. xx indicates factory programmed parts based on customer specific configuration. For more details, contact your local Cypress FAE or sales representative.

Package Diagrams

Figure 10. 24-pin QFN (4 × 4 × 0.55 mm) LQ24A (2.65 × 2.65 E-Pad (Sawn)) Package Outline, 001-13937



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Acronyms

Table 3. Acronyms Used in this Document

Acronym	Description
EMI	Electromagnetic Interference
FAE	Field Application Engineer
OE	Output Enable
PLL	Phase-Locked Loop
QFN	Quad Flat No-lead
SSC	Spread Spectrum Clock

Document Conventions

Units of Measure

Table 4. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
kΩ	kilo ohm
MHz	megahertz
µA	microampere
µs	microsecond
µW	microwatt
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY2542, Quad-PLL Programmable Spread Spectrum Clock Generator with Two-Wire Serial Interface and Frequency Select Document Number: 001-72951				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3378470	PURU	11/14/2011	New data sheet.
*A	3507333	PURU	01/30/2012	Removed SSON pin related information in all instances across the document. Replaced "I^2C Serial Interface" with "two-wire Serial Interface" in all instances across the document. Updated Logic Block Diagram.
*B	4580483	TAVA	12/11/2014	Updated Two-wire Serial Interface: Updated Figure 3. Updated Package Diagrams: spec 51-85203 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*C	5258614	TAVA	05/18/2016	Updated Two-wire Serial Interface: Updated Data Valid: Updated Figure 4. Added Serial I2C Programming Interface Timing Specifications. Removed "Two-wire Serial Programming Interface Timing Specifications". Updated Ordering Information: Updated Table 2: Updated part numbers. Updated Package Diagrams: Added spec 001-13937 *F (Figure 10). Updated to new template.
*D	5381451	PSR	08/06/2016	Updated Features: Replaced "24-pin (4 × 4 × 1 mm) QFN Package" with "24-pin QFN (4 × 4 × 0.6 mm) Package". Updated Ordering Information: Updated Table 2: Updated part numbers. Updated Package Diagrams: Removed spec 51-85203 *D.
*E	5778002	PSR	06/19/2017	Updated Features: Added one-time programmability. Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Pin Definitions: Updated details in "Description" column corresponding to pin numbers 2, 6, 10, 11, 13, 15, 17, and 20. Updated to new template.
*F	5955206	XHT	11/02/2017	Updated Logic Block Diagram. Updated DC Electrical Specifications: Updated details in "Max" column corresponding to V_{IL2} parameter. Updated details in "Max" column corresponding to V_{IH1} parameter. Updated details in "Min" column corresponding to V_{IH2} parameter. Updated to new template. Completing Sunset Review.

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